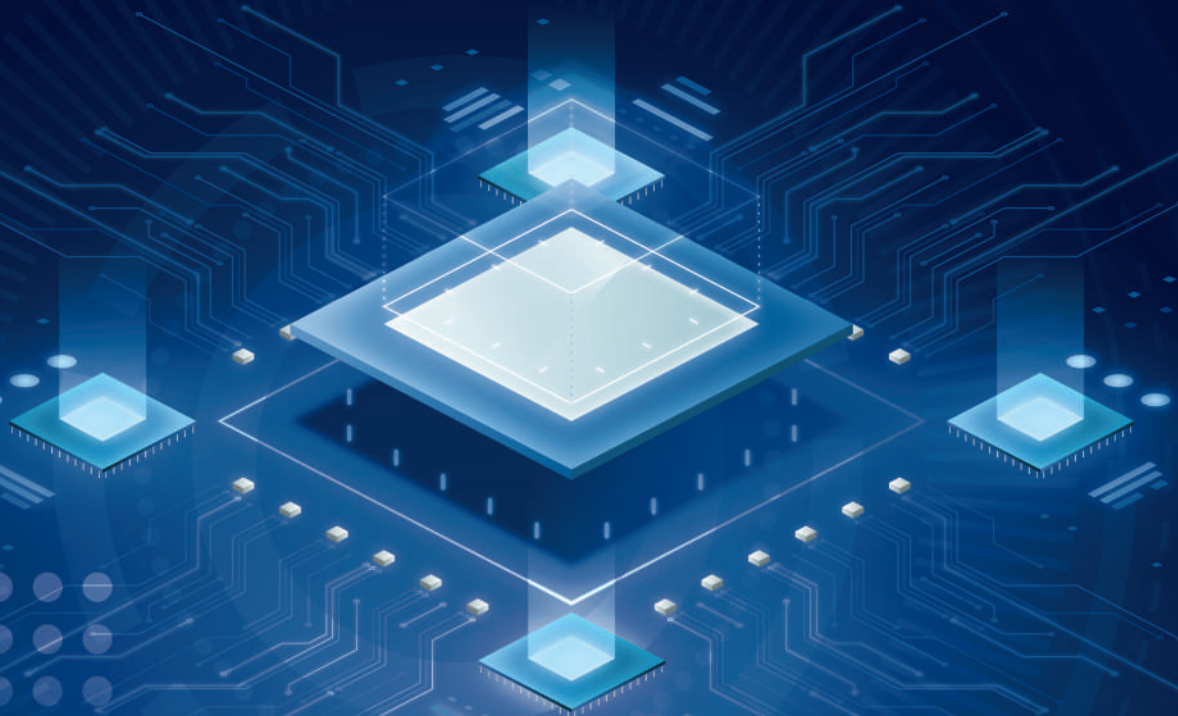


PAX SILICA: CHIP TO GRID

Opportunity to Lead in AI
and Semiconductors

May 2026
New Delhi, India



FOREWORDS

A Defining Inflection Point

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India stands at a defining inflection point. This paper arrives at a moment when policymakers, industry leaders, and bilateral partners seek greater value appropriation in 2030 from the projected \$1.75 trillion global semiconductor market.

The U.S.–India technology partnership has never been more consequential, and India’s entry into Pax Silica has architected a formalized engagement — a trusted, multilateral framework to secure the entire silicon stack, from critical minerals and chip design to AI deployment and grid infrastructure.

This paper advances policy thinking that semiconductor design, wafer fabrication, compute deployment, power delivery, and grid infrastructure are not parallel programs. These are deeply interdependent layers of a unified system. Policymakers working across ministries and regulatory bodies should internalize this system-level view.

India’s planned fabrication capacity with ₹1.6 lakh crore in investments under the India Semiconductor Mission (ISM) must be supplemented with deeper know-how. Equipment, advanced materials, and specialty chemicals confer deep competitive advantage and take decades to develop. ISM 2.0’s explicit focus on indigenous equipment and materials is the strategy. We urge that this be prioritized with the same urgency as fab expansion itself.

We urge energy policymakers to carefully consider that the electricity grid is the single largest constraint on India’s AI ambitions. Non-fossil sources represent over 52 percent of installed capacity. 748 gCO₂/kWh is India’s grid emission factor, reflecting continued coal dependence for baseload generation.

A strong, sustainable ecosystem requires energy efficiency across the computing stack and is the most immediate and scalable means of reducing infrastructure stress. Every watt saved in a chip is a watt the grid does not have to generate. This is not merely an environmental principle — it is a national economic one.

F O R E W O R D S

From Silicon to System: Why the Chip to Grid Imperative Matters Now

Mr. Sundeep Bajikar

CVP of Corporate Strategy, Applied Materials



Few industries have experienced the pace semiconductors have undergone, and fewer still carry the civilizational weight that silicon now does. At Applied Materials, we sit at the heart of this transformation: the equipment and materials that enable every node shrink, every advanced packaging innovation, and every breakthrough in power efficiency trace their origins to the physics and chemistry of semiconductor manufacturing. From that vantage point, the thesis advanced in this paper is not merely persuasive — it is urgent.

AI is not a software story. At its foundation, it is a materials and energy story. The next frontier of model capability will not be unlocked by code alone; it will be determined by transistor efficiency, interconnect density, thermal management of compute clusters, and the reliability of the grids that sustain them. This is why the Chip to Grid framework resonates so deeply with Applied's strategic view. The three pillars — a resilient energy grid, an energy-efficient computing supply chain, and globally competitive semiconductor markets — are not independent aspirations. They are a system, and systems either work together or fail at their weakest link.

India's position in this global system is one of genuine and growing consequence. With non-fossil sources now exceeding 52 percent of installed power capacity as of early 2026, the country is proving it can scale the infrastructure required for the AI age. The India Semiconductor Mission has matured into a strategic industrial engine, with ten projects and ₹1.6 lakh crore in cumulative investment now under execution. Over 38,000 GPUs deployed under the India AI Mission provide the sovereign compute capacity to turn design talent into industrial leadership. What this paper correctly identifies is the missing connective tissue: deliberate integration of grid infrastructure, energy-efficient compute, and semiconductor manufacturing into a coordinated national system rather than parallel programs.

Applied Materials has been a committed partner in India's technology journey, and the opportunity ahead is generational. Advanced packaging, power semiconductors for datacenters, and wafer fabrication equipment are domains where India can develop globally relevant capabilities — not as a late follower, but as a contributor to the next architecture of compute. The Pax Silica Declaration, signed on February 20, 2026, anchors the recommendations in this paper and provides exactly the kind of trusted, multilateral framework that serious semiconductor ambitions require.

I commend AMCHAM India and my colleagues at Applied Materials for the rigor and ambition reflected in this paper. The analysis is grounded, the recommendations actionable, and the moment is right. Leadership in AI will belong to those who build the full stack, from chip to grid.

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EXECUTIVE SUMMARY

Pax Silica: Chip to Grid

Artificial intelligence will be a defining general-purpose technology of the coming decade, shaping productivity, national competitiveness, and economic security. AI represents not only a technological leadership opportunity but a strategic instrument to raise productivity across a large and diverse economy.

As India enters this phase with several structural advantages, possessing one of the world's largest engineering talent pools, a rapidly expanding digital economy with over one billion users, and a policy framework that has mobilized capital and institutional support for both AI and semiconductors. These strengths place it among a small group of countries with credible ambitions to lead in AI-enabled growth.

At the same time, AI is fundamentally constrained by physical infrastructure. Advanced computing workloads require large, continuous, and reliable supplies of electricity. As global demand for AI compute expands, the availability, efficiency, and resilience of power systems will increasingly determine the pace at which countries can scale AI deployment.

This paper advances a central proposition: AI infrastructure must be planned and executed as a connected national system. Semiconductor design and manufacturing, compute deployment, research and innovation, and power generation and delivery are interdependent. Weakness in any one layer constrains the entire system; strength across all layers enables scale, efficiency, and resilience.

Important progress has been made across the semiconductor and AI stack, including in chip design, manufacturing initiatives under the India Semiconductor Mission, sovereign AI compute under the India AI Mission, and R&D financing through the Research Development and Innovation Fund. The next phase requires coordinated planning across these layers, with particular attention to energy efficiency and infrastructure readiness.

AI will only scale if the chip to grid stack is built as one system — because any weak layer becomes the constraint.

The paper proposes a holistic framework built on three mutually reinforcing pillars:

1. A stronger and more resilient electricity grid capable of supporting large-scale AI workloads.
2. An energy-efficient computing supply chain, from algorithms and system design to semiconductor equipment and materials.
3. The development of globally competitive semiconductor markets that translate infrastructure capability into sustainable economic growth.



This approach aligns with India's commitments under the Pax Silica Declaration, which emphasizes trusted, efficient, and secure silicon as a foundation of modern economic security. Taken together, these actions can convert the country's current momentum into durable leadership in AI and semiconductors.

THE AI OPPORTUNITY

Frontline of the Next Economic Era

The Case for AI Transition

Artificial intelligence is a foundational general-purpose technology that will materially influence economic growth, industrial competitiveness, and national security over the coming decade. AI represents a structural opportunity to raise productivity across a large and diverse economy, improve service delivery, and strengthen long-term economic resilience.

India enters this phase with several structural advantages, including one of the world’s largest pools of engineering talent, a rapidly expanding digital economy with over one billion users, and a policy framework that has mobilized capital and institutional support for AI and semiconductors. However, AI is fundamentally constrained by physical infrastructure, particularly electricity. Global datacenter electricity demand is projected to exceed 1,000 terawatt-hours by 2027, driven primarily by the growth of AI workloads.¹ Each successive generation of models and chips increases computational density, enables more applications and usage models, and ultimately leads to higher total power consumption.

The electricity grid remains in transition. While non-fossil capacity (Figures 1, 2) exceeded 52 percent of installed capacity as of January 2026, the system continues to carry a relatively high emissions intensity, reflecting ongoing dependence on coal for baseload generation.

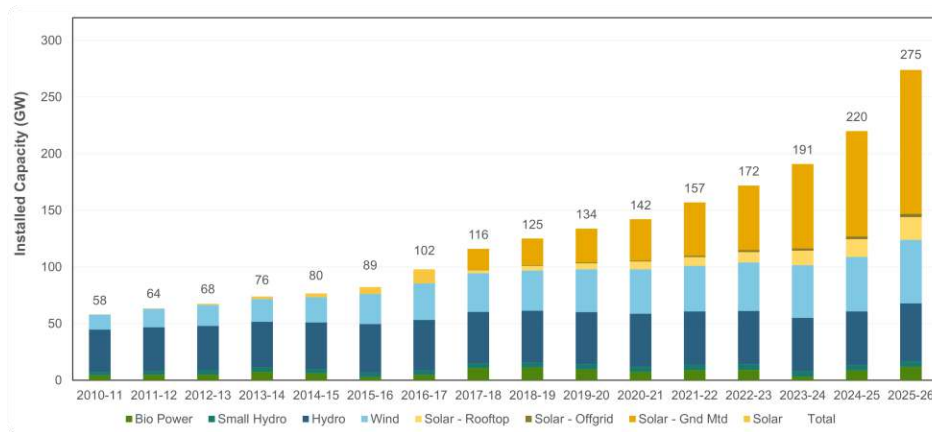


Figure 1. India’s Renewable Energy Progress

Source: India’s Climate and Energy Dashboard (ICED), NITI Aayog — MNRE & CEA. [5]

¹ International Energy Agency, *Electricity 2024* (2024); Applied Materials, *Sustainable Energy Abundance for AI* (2025). See References 7 and 1.

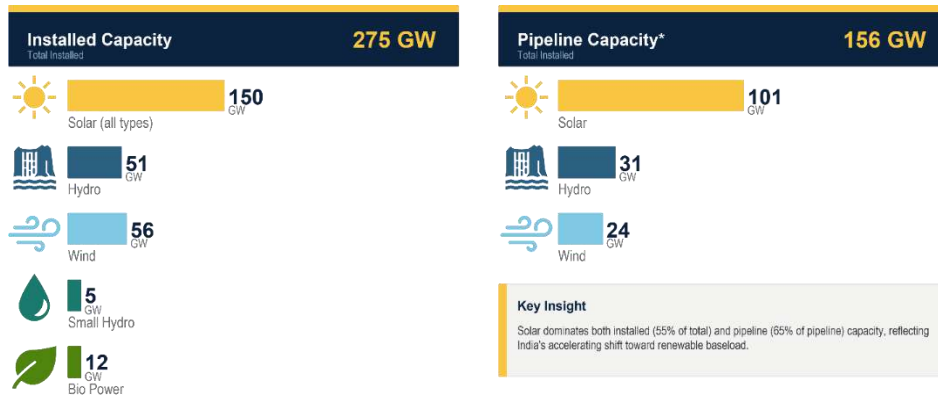


Figure 2. India's Renewable Energy Capacity

Source: India's Climate and Energy Dashboard (ICED), NITI Aayog — MNRE & CEA · FY 2025–26 data is till 31st March 2026. [5]

These dynamics require AI infrastructure to be treated as a connected national system. Semiconductor design, manufacturing equipment, fabrication operations, compute deployment, power delivery, and the electricity grid function as interdependent layers. Weakness in any one layer constrains the performance of the system as a whole.

It is important to acknowledge the current status and the potential ahead, starting with the semiconductor stack.

THE SEMICONDUCTOR STACK

The Five Layers India Is Building

Design

Chip design represents one of the most mature and globally integrated capabilities. Indian engineering teams are actively contributing to designs at advanced process nodes, including 2nm geometries. Over 100 fabless chip design firms now operate in the country. Free access to advanced electronic design automation tools through academic institutions has strengthened the talent pipeline and aligned early-stage training with industry-relevant workflows. The engineers learning on these tools today are the ones who will design the energy-efficient chips the world needs tomorrow.

Manufacturing

The India Semiconductor Mission (ISM) marks a transition from project-based manufacturing incentives to a broader ecosystem-oriented industrial strategy. As of April 2026, ten semiconductor projects across six states, with cumulative investment of approximately ₹1.6 lakh crore, are under execution. The next phase of ISM places explicit emphasis on high-value segments, including indigenous equipment development, advanced materials, specialty chemicals, and full-stack design intellectual property. This focus reflects global experience that long-term competitiveness depends on process capability and equipment know-how, not fabrication capacity alone.

Compute

The India AI Mission has deployed over 38,000 GPUs at globally competitive rates, enabling access to advanced compute for startups, researchers, and public-sector use cases. To date, approximately 190 AI projects have progressed from approval to deployment, establishing early demand for sovereign compute capacity. The broader AI ecosystem is reinforced by a large base of 1,800+ Global Capability Centers (GCCs) and a skilled workforce exceeding six million professionals across technology and AI-related functions.

Research and Innovation

The Research Development and Innovation Fund (RDIF), administered by the Department of Science and Technology, provides a long-term mechanism to de-risk private investment in strategic and deep-technology domains. With a total outlay of ₹1 lakh crore, RDIF addresses a longstanding gap in financing projects at higher technology readiness levels, particularly in semiconductors, AI-enabled systems, and advanced infrastructure technologies.

Critical Minerals

The National Critical Mineral Mission is actively exploring 1,200 sites. Rare earth corridors in Odisha and Kerala are being developed to move from raw ore export into midstream processing. The ₹1,500 crore Urban Mining incentive scheme, announced in October 2025, complements this effort. India's growing consumer electronics market becomes a domestic source of recoverable materials, including semiconductor-grade gallium, indium, and rare earths.

Collectively, these capabilities provide an operating position that few countries possess: functional depth across design, manufacturing, compute, research, and critical inputs. The remaining challenge is not the creation of additional capacity, but the integration and coordinated scaling of existing systems.

THE HOLISTIC VIEW FOR AI

Three Pillars, One System

Why a Systems Approach Is Required

AI workloads are characterized by high density, continuous operation, and limited tolerance for interruption. As a result, computational efficiency, fabrication capability, and grid resilience increasingly determine national scaling capacity.

When any one layer is weak, the whole system slows down. A world-class chip design is wasted if the fab cannot produce it. A state-of-the-art fab is wasted if the grid cannot power it cleanly. A clean grid is wasted if the chips drawing from it are inefficient.

The opposite is also true. When every layer is strong, each one makes the others better. An efficient chip reduces the load on the grid. A cleaner grid lowers the carbon cost of every wafer made. New semiconductors, in turn, make the grid smarter and cleaner. The layers reinforce each other.

A holistic approach rests on three pillars. They are the same three pillars that shaped Applied Materials' 2025 global analysis of sustainable energy and AI. They apply with equal force.

The Three-Pillar Framework

Pillar I is a cleaner, stronger grid. The grid is the single largest source of emissions for any AI operation. It is also the single biggest constraint on how fast AI can grow. The grid is improving. With the right investments, it can support a much larger AI build-out at a much lower carbon cost.

Pillar II is an energy-efficient computing supply chain. This covers the full stack, from algorithms and software to chip and system design, to wafer fab equipment and fabs. The semiconductor industry is shifting to a new playbook. New transistor architectures, new memory designs, and new advanced packaging approaches are delivering large efficiency gains. Materials engineering is what makes these gains possible.

Pillar III is monetizing new global semiconductor opportunities, from chips to the wafer fab equipment supply chain. A cleaner grid and energy-efficient AI computing catalyze new market opportunities at a sustainable cost advantage. AI computing processors, memory, storage, power semiconductors, and the wafer fab equipment supply chain used to make these semiconductors are all global markets on an attractive growth path.

AI ambitions in the global context require strong partnerships on all three pillars to realize a holistic system architecture.

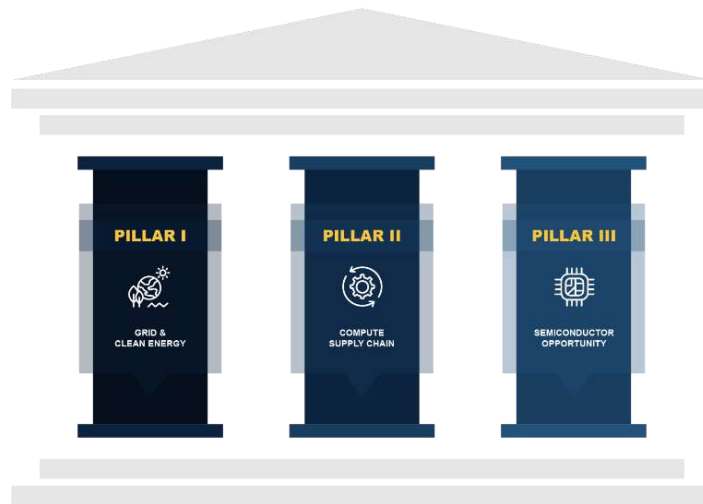


Figure 3. Three-Pillar Framework

Source: Applied Materials, Corporate Strategy & Marketing

PILLAR I

A Cleaner, Stronger Grid for AI Ambitions

K E Y A N A L Y T I C A L P O I N T S

- Grid capacity and reliability set the ceiling on AI scale.
- Generation mix, transmission, and distribution reliability will govern AI expansion over the next two decades.
- A cleaner, stronger grid enables more AI compute and lowers the carbon cost of the full chip to compute stack.

The electricity grid constitutes the principal physical constraint on large-scale AI deployment. Decisions related to generation mix, transmission capacity, and distribution reliability will shape the feasible pace of AI expansion over the next two decades. Every chip, every fab, and every datacenter runs on the grid. The cleaner the grid, the lower the carbon cost of everything built on top of it. The stronger the grid, the more AI capacity can be added without hitting a wall.

Where We Stand

The grid is in transition. Non-fossil energy capacity crossed 52 percent of installed capacity in January 2026. The direction of travel is right.

At the same time, the grid's emission factor is approximately 748 grams of CO₂ per kilowatt-hour. This is higher than many other large economies. It reflects a system that still depends on coal for a large share of generation, even as solar, wind, hydro, and nuclear capacity grow.

This gap between installed capacity and actual emissions matters. Adding more renewable projects is necessary but not sufficient. India must also modernize how electricity moves from where it is generated to where it is used.

Global Energy Scenario

With the adoption of AI, the technology share of electricity consumption is set to rise sharply over the next 10 to 20 years. It is estimated that electricity consumption by technology applications will increase from approximately 10 percent in 2021 to 25 percent in 2030 and 50 percent in 2050.

While AI is a significant driver of this growth, the transition to electric vehicles, the move to digital, and the proliferation of IoT all contribute to expanding technology electricity consumption.

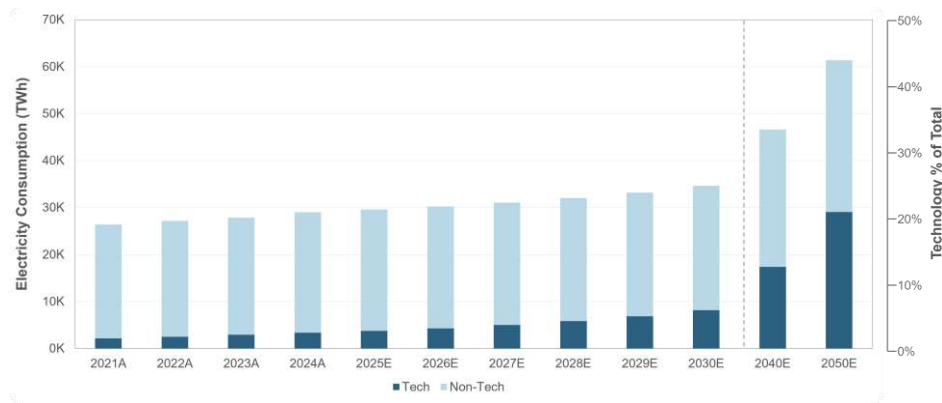


Figure 4. Global Electricity Consumption: Technology vs. Non-Technology, 2021A–2050E

Source: Applied Materials Strategy & Market Intelligence. Adapted from Sustainable Energy Abundance for AI (2025). [1]

As AI adoption increases, the mix of electricity consumption between traditional and AI datacenters will shift. Over the next several years, AI datacenters will be the biggest driver of electricity usage in the datacenter category.

The 3 Levers of a Strong Grid

From a policy perspective, three levers require coordinated attention: generation scale-out, transmission modernization, and intelligent distribution. Progress on only one dimension is not sufficient for long-term success.

Generation scale-out. We need more electricity, and more of it from clean or carbon-free sources. Solar, wind, hydro, nuclear, and natural gas all have a role to play. A diverse generation mix is more stable than one that depends on any single source. The continued build-out of solar capacity is important. So is the serious consideration of nuclear, including small modular reactors, which can provide steady baseload power near datacenters and fabs.

Transmission modernization. Clean electricity is only useful if it can reach the places that need it. Many renewable projects are stranded because transmission lines and substations have not kept up. We should prioritize upgrades to high-voltage lines, regional interconnects, and control systems. This is where much of the value of new generation is either captured or lost.

Smart distribution. The last layer is the one closest to the user. Digital sensors, smart meters, and AI-driven load management let the grid respond to demand in real time. They reduce waste. They improve reliability. And they create a natural fit between the grid's needs and AI's ability to optimize complex systems.

Locating Fabs and Datacenters Near Clean Power

Where a fab or datacenter is built matters almost as much as how it is run. A fab located in a region with a high share of clean power inherits that clean profile. A fab in a coal-heavy region inherits that too, regardless of how efficient its internal operations are.

There is strong regional variation in grid cleanliness. States with more hydro, solar, or nuclear generation offer a lower-carbon starting point for new fabs and datacenters. Policy can help by making

this variation visible and by offering incentives for siting near clean power. Water also belongs in this conversation. Fabs and datacenters use significant amounts of water, and regions that face water stress are also where energy systems become fragile under drought. Planning fab and datacenter locations with both electricity and water in mind reduces risk for investors and for the country.

What This Means

AI workloads are demanding. A training run may not be paused when the grid is stressed. Inference cannot wait for a cloudy day to pass. The grid therefore needs to be built for the harder case, meaning abundant, clean, and reliable power delivered at the moments and places AI needs it.

The good news is that we are early enough in the AI build-out to make grid choices with AI in mind. Many other countries are having to retrofit their grids mid-stream. A stronger, cleaner grid is not only an environmental goal. It is the foundation that allows every other part of the AI and semiconductor ambition to work.

PILLAR II

An Energy-Efficient Computing Supply Chain

K E Y A N A L Y T I C A L P O I N T S

- Efficiency gains increase AI capability per watt, easing grid constraints.
- The AI ceiling depends on executing the efficiency stack (architecture/3D/packaging/materials + software) and linking design strength to equipment/process depth.

The End of Easy Gains

For five decades, the semiconductor industry rode a single trend. Transistors got smaller. Chips got faster. Power went down. Cost per transistor fell. This was classic 2D scaling — the Moore's Law era — and it powered the PC and mobile eras.

That era is over. Classic scaling has slowed dramatically. Between 1986 and 2003, chip performance improved at about 50 percent per year. Since 2015, the rate has dropped to around 3.5 percent per year. This does not mean progress has stopped. It means progress now requires a new playbook.

The New Playbook

Future performance gains rely on a combination of architectural innovation, three-dimensional integration, advanced packaging, and materials engineering. These shifts elevate the importance of process equipment, materials science, and design-for-manufacturability.

New chip architectures like GPUs and custom accelerators are designed to match the workloads. 3D design techniques stack devices vertically. Novel materials change how electrons move through a transistor. New methods continue shrinking feature geometries where it still makes sense. Advanced packaging connects chips together in tighter, faster, more efficient ways.

Each of these alone delivers a modest gain. Combined, they can deliver performance improvements of up to 2,500 times, exceeding what classic 2D scaling alone would have produced by orders of magnitude. This is where the industry is headed, and where the design and manufacturing ecosystem should aim.

Materials Engineering is the Enabler

Every item in the new playbook comes back to the same discipline: materials engineering.

At the nanometer scale, the behavior of a chip is decided by a handful of atomic layers. Gate-All-Around (GAA) transistors, the successor to FinFET, deliver a 25–30 percent improvement in energy efficiency. GAA is built on five carefully chosen materials in a channel with layers one to two nanometers thin.

Backside Power Delivery moves power routing to the underside of the wafer, freeing up space on top and reducing losses. 3D NAND stacks over 100 layers of materials with extreme precision. Each of these inflections depends on the ability to deposit, shape, and modify materials at the atomic scale.

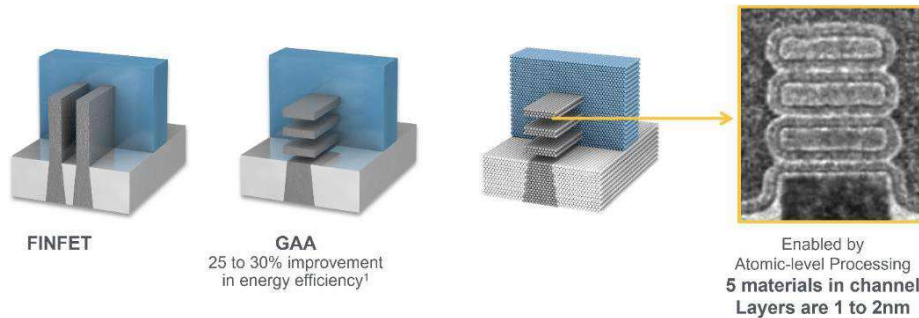


Figure 5. Critical device inflections enabled by Materials Engineering

Source: TSMC; Applied Materials. Reproduced from Sustainable Energy Abundance for AI (2025). [1, 8]

This is specialized work, and it is one of the deepest capabilities in the industry. As chip features move from nanometers to angstroms, materials behave in new ways. Surface properties begin to dominate bulk properties. Getting this right is a hard and narrow problem, and it is one of the reasons the ambition to reach 3nm and 2nm fabrication capability is serious and realistic.

What This Means

We have one of the strongest design layers in the world. Indian engineers are already working at 2nm. Over 100 fabless firms operate in the country. Students have free access to world-class design tools. The talent that will shape the new playbook is in India.

What the country now needs is to connect that design strength to a deep, local capability in manufacturing equipment and processes. This is the quietest part of the stack. This is the most strategic part of the stack. Fabs can be built. Equipment know-how takes decades to develop. ISM 2.0's focus on indigenous equipment, advanced materials, and specialty chemicals is exactly the right approach.

Software and system design are also important. Workloads that are written well use less power than workloads that are not. Systems designed with efficiency in mind extract more compute from every watt. These are strengths we can build quickly, and they improve the return on every chip the country designs and every fab it builds.

The energy-efficient computing supply chain is not one project. It is a portfolio of capabilities, stacked on top of each other. We have the start of every layer. Connecting them is the next move.

Pillar II concludes that as 2D scaling slows, AI scale depends on end-to-end efficiency, because each watt saved anywhere in the stack directly increases deployable compute under fixed grid limits.

PILLAR III

New Global Semiconductor Opportunities

K E Y A N A L Y T I C A L P O I N T S

- Grid + efficiency advantages unlock competitiveness across high-growth chip markets.
- Multiple \$B markets are expanding through 2030 (DC power, renewables, smart infra, charging, grid transformation; total semis ~\$1.6–\$1.75T).
- Capturing these markets deepens silicon/equipment base, compounding national AI capability.

The combination of infrastructure readiness and efficiency enables participation in several rapidly growing global semiconductor markets, including AI accelerators, power electronics, renewable energy systems, smart infrastructure, and grid modernization technologies. With the country's design talent, manufacturing build-out, and growing equipment ecosystem, is well placed to compete in every one of them.

AI Computing Hardware

AI computing is the engine of demand for advanced semiconductors. GPUs, custom AI accelerators, high-bandwidth memory, and advanced storage are all growing quickly. Every major cloud provider is now designing its own custom chips to extract more performance from every watt.

The trajectory is steep and the opportunity is large. Over the last five generations of GPUs, floating-point performance has increased by roughly 500 times. Custom accelerators announced by Google, Amazon, Microsoft, Meta, and others show no sign of slowing. This is a market India's design talent is already plugged into, and one the fabs can increasingly serve. AMD CEO Lisa Su recently raised her estimate for the total addressable market of chips for datacenters to \$1 trillion by 2030².

Power Semiconductors for Datacenters

Datacenters are full of chips that do not perform computing. They handle power conversion: stepping voltages up and down, delivering clean power to processors, and managing thermal loads.

This is a fast-growing market on its own. We estimate the market for datacenter power semiconductors could reach \$9 billion by 2030. Gallium nitride (GaN) and silicon carbide (SiC) are taking share from traditional silicon, because they deliver higher efficiency and smaller footprints. These are new materials with new process requirements, and the equipment and know-how to make them are still concentrated in a few places. That is an opening for India.

² Cherney, Reuters (2025). See Reference 2.

Semiconductors for Renewable Energy

Every solar panel, every wind turbine, and every battery system needs semiconductors. As the share of renewables on the grid grows, so does the chip content in each megawatt of generation.

It is estimated the market for semiconductors in renewable generation is on track to reach around \$23 billion by 2030. SiC is the workhorse material here. Building out solar capacity aggressively, there is both a domestic pull and a global supply opportunity.

Semiconductors for Smart Infrastructure

Smart meters, smart sensors, heat pumps, and building energy management systems all run on chips, and demand for them is scaling with the grid's own modernization.

It is estimated smart infrastructure is on track to drive around \$19 billion in semiconductor revenue by 2030. This is a market that rewards volume, reliability, and cost, a profile that would play to India's strengths as a manufacturer.

Semiconductors for EV Charging and Grid Integration

Electric vehicles do not only consume power. With vehicle-to-grid (V2G) technology, they can return power to the grid when it is needed. This turns every EV into a small, flexible grid asset.

It is estimated charging infrastructure alone could drive around \$4 billion in semiconductors by 2030. V2G and vehicle-grid integration platforms extend that opportunity considerably. It is estimated the grid transformation market, combining generation, transmission, and distribution, is on track to reach \$50 billion in semiconductor revenue by 2030.

Wafer Fab Equipment, the Deepest Opportunity

Capability in wafer fabrication equipment and sub-systems represents a particularly strategic opportunity, given the sector's critical importance and concentrated global supply chains. Every chip in every category above is made on equipment designed and built by a small number of companies. The equipment is complex, precise, and deeply dependent on materials science. This is where value in the industry concentrates, and where supply chains are thinnest.

ISM 2.0's focus on indigenous equipment, advanced materials, and specialty chemicals is an investment in exactly this layer. Building equipment capability creates both a domestic advantage and an export opportunity. The global fab build-out of the next decade will need more equipment, not less, and the countries that host equipment capability will sit at the center of the industry's value chain.

What This Means

The global semiconductor market is large and growing. McKinsey forecasts semiconductor industry revenues to reach \$1.6 trillion by 2030³. IDC's base case projects semiconductor revenues reaching \$1.75 trillion by 2030⁴. Semiconductor industry forecasts have been revised up significantly over the last year. Wafer fab equipment is the key enabler for semiconductors.

These markets reward the things we have. Strong design. A growing fab ecosystem. An expanding equipment and materials capability. A growing domestic demand base that can anchor exports.

Growth does not come from a single bet. It comes from competing across the portfolio, and doing so at a sustainable cost advantage. That advantage is built on top of the first two pillars: a cleaner grid and an efficient computing supply chain. The three pillars reinforce each other and deliver compounding growth.

³ Wiseman et al., McKinsey & Company (2026). See Reference 3.

⁴ Janukowicz & Turner, IDC Research (2026). See Reference 4.

POLICY AND PARTNERSHIPS

Building the Pax Silica Framework

International experience demonstrates that advanced semiconductor ecosystems emerge through sustained collaboration across design, equipment, materials, and manufacturing. Strategic partnerships are therefore a structural requirement rather than a transitional phase⁵.

India's semiconductor goals are serious. Reaching 3nm and 2nm fabrication capability by 2030 to 2035 is a credible target, and ISM 2.0 is funding the right layers, including equipment, materials, and specialty chemicals, rather than basic assembly.

Hitting those targets is a technical problem more than a financial one. It calls for specialized tools, refined processes, trained engineers, and a dense web of supplier and research relationships. No country has built advanced fab capability alone. Every leading semiconductor nation, whether the United States, Taiwan, South Korea, or Japan, got there through close collaboration with global equipment, materials, and design partners.

Semiconductors are the deepest, most globally distributed supply chain ever built. The country's advantage will come from plugging into that structure at the right points, with the right partners, on the right terms.

Where Partnerships Add the Most Value

Chip design and R&D. Fabless firms, research institutions, and universities can go further, faster, with close ties to the equipment and materials companies whose tools define what is manufacturable. Design for manufacturing and design for efficiency are team sports. The earliest design choices shape how efficient a chip can ever be.

Fab equipment and process technology. Moving to advanced nodes means integrating hundreds of specialized tools into working process flows. The tools themselves are one part of the challenge. The integration know-how, meaning the accumulated judgement of which recipes work, which materials fail, and which inflections are ready, is the harder part, and it takes years to transfer.

Workforce development. The global semiconductor industry is short roughly one million skilled workers. We have the talent pipeline to close a large part of that gap. Turning raw talent into world-class process and equipment engineers calls for training programs, joint research centers, and engineer exchanges with companies that do this work at scale.

Equipment supply chain. ISM 2.0's focus on equipment R&D is a strategic choice. Building domestic capability in components, subsystems, and eventually integrated tools is faster when it happens alongside established equipment companies who can share standards, qualify suppliers, and open export channels.

⁵ Thadani & Allen, CSIS (2023). See Reference 9.

The Pax Silica Context

India's signing of the Pax Silica Declaration on February 20, 2026 makes these partnerships timelier. Pax Silica is built on the idea that the trusted, efficient, and sustainable silicon stack is core to modern economic security. Deep technical collaboration across borders, from design to equipment to the grid, is how that idea becomes real.

The initiative operationalizes a stated “economic security is national security” consensus, treating secure, diversified access to the silicon stack as a prerequisite for national power, prosperity, and sovereignty in an AI-driven world⁶. The core objective of Pax Silica is to enable partnerships that secure global technology supply chains, address AI supply chain opportunities and vulnerabilities, and explore joint investment. Another is to protect sensitive technologies and build trusted digital infrastructure. The long-term benefit of Pax Silica will be to unite economies hosting advanced technology companies and unleash the economic potential of the new AI age, driving AI-powered prosperity across partner nations. We are well positioned on all fronts.

Key instruments include joint supply chain mapping, co-investment, and industrial park projects, protection of sensitive technologies and critical infrastructure, and a proposed \$250 million Pax Silica Fund to catalyze larger public–private investments.

“We recognize that the technological revolution in AI is accelerating, increasingly reorganizing the world economy, and reshaping global supply chains. We believe that economic value and growth will flow through and across all levels of the global AI supply chain, driving historic opportunity and demand for energy, critical minerals, manufacturing, technological hardware, infrastructure, and new markets not yet invented.”

— Pax Silica Declaration, U.S. Department of State (2026) [6]

How Pax Silica Can Enable Chip to Grid Ambitions

Strategic Market Access and Investment

As a member of the United States–led Pax Silica coalition, we are embedded in a trusted network that seeks to secure the entire “silicon stack”, from critical minerals and semiconductor fabrication to AI infrastructure and deployment. This positioning can unlock preferential access in coalition markets to demand, technology, and finance, allowing commercial partnerships to become strategic security assets. If aligned with domestic schemes such as the India Semiconductor Mission and the Design Linked Incentive (DLI) program, Pax Silica can help firms move up the value chain into high-value chip design, power electronics, and AI systems integration, instead of remaining confined to assembly.

⁶ U.S. Department of State, Pax Silica Declaration (2026). See Reference 6.

Anchoring India's Position in the Global South

Pax Silica reinforces the stated objective of combining strategic autonomy with deeper integration into trusted technology coalitions. It allows India to participate in shaping emerging norms on secure technology supply chains, export controls, and AI governance within a grouping explicitly framed around open, democratic societies. We are uniquely placed to interpret and adapt these norms for the wider Global South, offering secure, affordable and development-oriented chip to grid solutions that draw on the country's experience with digital public infrastructure and inclusive AI initiatives. Coalition mechanisms can de-risk access to critical minerals and advanced manufacturing equipment, facilitate the deployment of secure AI servers and accelerators in datacenters, and promote joint development of power electronics and grid-edge devices.

Vertical Integration of Manufacturing

The 'Make in India' and Production Linked Incentive (PLI) schemes have already made India a major electronics and mobile manufacturing hub. Electronics production has risen sharply over the last decade, but domestic value addition still hovers around 18–20 percent and is concentrated in assembly. By anchoring within a trusted semiconductor and AI ecosystem, Pax Silica can accelerate joint R&D, technology transfer and localization of components, sub-modules and capital equipment, allowing the country's industry to move up the manufacturing value chain into chip design, advanced packaging, power electronics and complex systems integration. The policy priority will be to align coalition opportunities with domestic incentives and skilling so that India captures higher-value segments rather than remaining a volume platform for others' IP.

Furthering Pax Silica

Market Scale as a Platform for Innovation

India is now one of the world's largest and fastest-growing markets for electronics, with total electronics consumption estimated at around ₹17 trillion in FY 2025–26, driven by mobile phones, consumer devices and industrial electronics. Under the Production Linked Incentive (PLI) scheme for Large Scale Electronics Manufacturing, mobile phone production has risen more than 28-fold in value over the past decade and exports have grown over 100-fold, making India the world's second-largest mobile phone manufacturer and a net exporter. Pax Silica can align this expanding domestic market with trusted supply chains and advanced technologies from partner countries, allowing it to leverage market dynamics to get access to technology transfer, co-development and local value addition. By deliberately steering a portion of coalition demand for components, sub-assemblies and finished products through domestic facilities, the government can turn the market size into a platform for innovation – supporting indigenous standards, local IP creation and experimentation with new chip-to-system architectures at scale. Eventually, every electronic device connects into a grid. Large markets which push for energy-efficient devices and frameworks across billions of small and large electronic devices change the lens of grid efficiency from origination to source.

Scaling STEM Talent and Chip Design

We already account for approximately 20 percent of the world's semiconductor design engineers. The India Semiconductor Mission's Design Linked Incentive (DLI) and futureDESIGN initiatives explicitly aim to convert this human-capital advantage into a vibrant ecosystem of domestic fabless companies and IP owners across applications such as automotive, mobility, communication, computing and power electronics. Participation in Pax Silica can amplify this effort by opening structured pathways for joint R&D, shared EDA and prototyping infrastructure, and cross-border design teams working on secure, export-compliant solutions for coalition markets. A coordinated talent strategy, spanning higher education, skilling, and mobility arrangements with partner countries can enable engineers to move from primarily implementing architectures defined elsewhere to conceiving and owning full-stack chip and system designs, thereby anchoring at the innovation frontier of the semiconductor value chain.

CONCLUSIONS

Closing the System Loop

The core components required to participate meaningfully in the next phase of AI-driven growth are assembled. The country possesses advanced design talent, early-stage manufacturing capacity, sovereign compute infrastructure, and mechanisms to finance strategic innovation.

The decisive factor now is coordination. AI infrastructure must be governed as an integrated system spanning silicon, compute, power, and institutions. Incremental gains within individual programs will not substitute for system-level alignment. Three priorities follow.

First, power systems must be strengthened and planned with AI workloads in mind. Generation, transmission, and distribution should advance together, with siting, water, and reliability treated as design inputs rather than afterthoughts.

Second, an energy-efficient computing supply chain should be treated as a strategic objective. From algorithms and software to chip design, wafer fab equipment, and fab operations, every layer offers leverage. Materials engineering is the common thread that makes the new semiconductor playbook possible.

Third, we should convert infrastructure capability into sustained participation in global semiconductor markets. The opportunities in AI hardware, datacenter power, renewables, smart infrastructure, and the wafer fab equipment supply chain reward exactly the capabilities being built.

Engagement with the Pax Silica framework reinforces this approach by enabling trusted partnerships, shared standards, and coordinated investment across critical technologies. Used effectively, it can reduce execution risk while increasing strategic relevance in global AI and semiconductor ecosystems.

In the AI era, advantage accrues to countries that run the chip to grid stack as one integrated system — because bottlenecks set hard ceilings and coherence compounds scale.

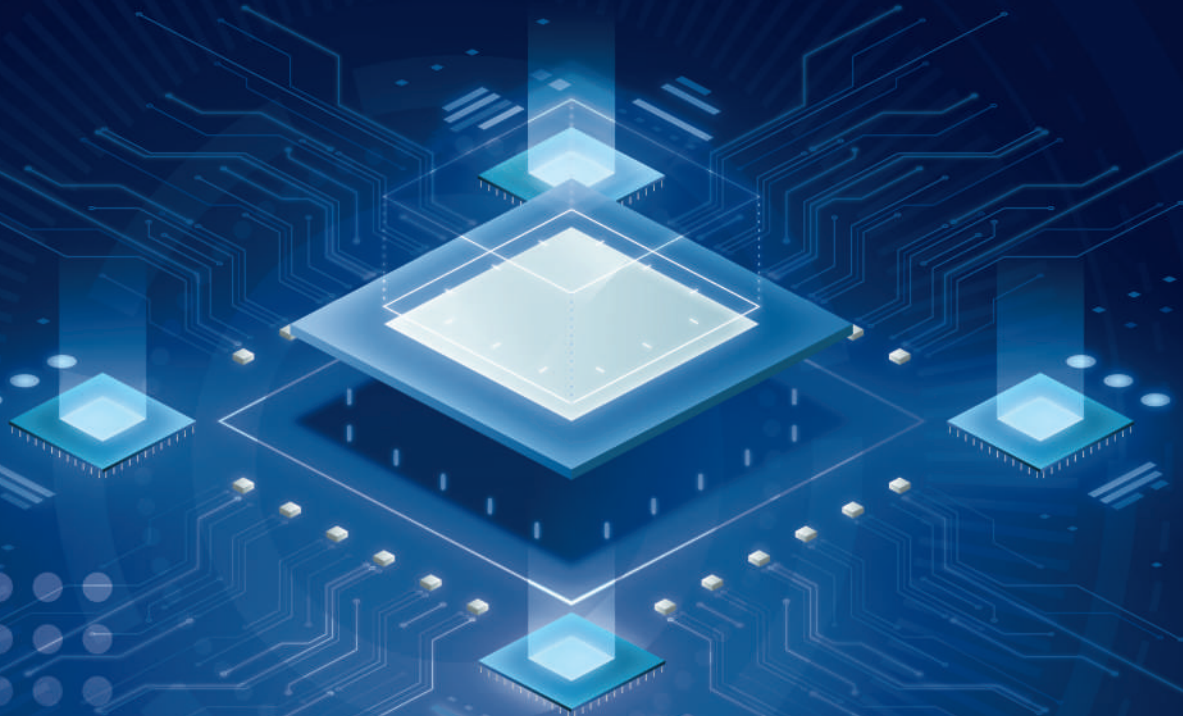
The opportunity is significant but time-bound. Countries that integrate technology, infrastructure, and institutions into coherent operating systems will define the next phase of economic and technological leadership. Having established the necessary foundations, the task now is disciplined execution, coordinated planning, and timely scale.

About AMCHAM India

The American Chamber of Commerce in India (AMCHAM India) is the leading apex chamber of U.S. industry in India. Established in 1992, AMCHAM has over 400 U.S. companies as members and plays a pivotal role in fostering strong ties between the U.S. and India. The incumbent U.S. Ambassador to India is the Honorary President of AMCHAM. The chamber enjoys a close relationship with the U.S. Embassy and complete support in fulfilling its objectives. Country Heads of leading U.S. companies constitute the elected national executive board. The chamber's mission is to assist member companies to succeed in India through advocacy, information, networking and business support services. Headquartered in New Delhi, AMCHAM extends its influence through regional chapters in Bengaluru, Chennai, Hyderabad, Kolkata, Mumbai and Pune.

About Applied Materials

Applied Materials, Inc. (Nasdaq: AMAT) is the leader in materials engineering solutions that are at the foundation of virtually every new semiconductor and advanced display in the world. Headquartered in Santa Clara, California, the company employs around 33,000 people across 120 cities globally and serves chipmakers across the United States, China, Korea, Taiwan, Japan, Southeast Asia, and Europe with equipment, services, and software spanning deposition, etch, modification, metrology, inspection, and advanced packaging. Its tools are central to enabling the leading-edge logic, high-bandwidth memory, and heterogeneous integration that power the AI era — making Applied a foundational supplier to the global buildout of AI infrastructure and next-generation compute. In India, Applied has a deep, multi-decade presence across R&D, engineering, and manufacturing, and is a committed partner in strengthening the country's semiconductor ecosystem.



GLOSSARY

Acronyms and Key Terms

AI	Artificial Intelligence
CEA	Central Electricity Authority
DLI	Design Linked Incentive (scheme)
RDIF	Research Development and Innovation Fund
GCC	Global Capability Center
HBM	High-Bandwidth Memory
GAA	Gate-All-Around (transistor)
GaN	Gallium Nitride
EV	Electric Vehicle
DPI	Digital Public Infrastructure
TWh	Terawatt-hour
ICAPS	IoT, Communications, Auto, Power, Sensors
ISM	India Semiconductor Mission
MNRE	Ministry of New & Renewable Energy
PLI	Production Linked Incentive (scheme)
ICED	India's Climate and Energy Dashboard
GPU	Graphics Processing Unit
NAND	NAND Flash Memory
EDA	Electronic Design Automation
SiC	Silicon Carbide
V2G	Vehicle-to-Grid
IoT	Internet of Things
kWh	Kilowatt-hour

Disclaimer

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